ABSTRACT OF THE DISCLOSURE

Flash memory is rapidly decreasing in price. There is a demand for a new memory system that permits size reduction and suits multiple-value memory. A flash memory of AND type suitable for multiple-value memory with multiple-level threshold values can be made small in area if the inversion layer is utilized as the wiring; however, it suffers the disadvantage of greatly varying in writing characteristics from cell to cell. Another promising method of realizing multiple-value memory is to change the storage locations. This method, however, poses a problem with disturbance at the time of operation. The present invention provides one way to realize a semiconductor memory device with reduced cell-to-cell variation in writing characteristics. The semiconductor memory has a source region and a drain region, which are formed parallel to each other, and an assist electrode which is between and parallel to the source and drain regions without overlapping, so that it uses, at the time of writing, the assist electrode as the assist electrode for hot electrons to be injected at the source side and it uses, at the time of reading, the inversion layer formed under the assist electrode as the source region or the drain region.